Amendments to the Specification:

Please amend the paragraph bridging pages 4-5 as follows:

In accordance with embodiments of the present invention, FIG. 3 shows an exemplary processor system architecture 300 for reducing power consumption by rapidly reducing the clock frequency for the processor system during these periods of high-power spikes and then resuming regular (non-reduced) clock frequency after the high (danger) temperature period has completed. The intercoupled processor architecture 300 includes processor component (die) thermal sensor 335, intercoupled to frequency reduction circuit 305, ~~phase-locked loop (PLL) circuit 310 intercoupled to frequency reduction circuit 305,~~ logic circuit 315 intercoupled to PLL (phase-locked loop) circuit 310 and frequency reduction circuit 305, and may optionally include inverter 328 intercoupled to logic circuit 315 for outputting a stable timing signal (the clock frequency signal – clk) 330 for the processor system 300. Frequency reduction circuit 305 may include a counter 313 (e.g., four-bit circular counter) and enabling control logic 312.